transistors and a second level of transistors made of single crystal silicon disposed about a Z-dimension of said semiconductor film.

22. (Amended) The apparatus of claim 14 having a first level of transistors and a second level of transistors made of single crystal silicon [in the] disposed about a Z-dimension.

Please add the following new claims.

--23. (New) The apparatus of claim 14, further comprising:

means for removing the damaged surface from the first substrate.--

--24. (New) The apparatus of claim 23, further comprising:

a second substrate with a metal film formed thereon, said second substrate bonded with the metal film to said semiconductor film of said first substrate.--

REMARKS

Claims 14 and 17-22 have been examined and claims 14 and 17-22 remain in the Application. Claims 23 and 24 have been added. Claims 20 and 21 are rejected under 35 U.S.C. § 102(e). Claims 14 and 17-22 are rejected under 35 U.S.C. § 103(a).

A. 35 U.S.C. § 102(e): Rejection of Claims 20-21

The Examiner rejects claims 20 and 21 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,744,866, issued to Horiba ("*Horiba*"). Claim 20 describes a first oxide film formed on a substrate. Claim 20, line. 3. A metal film is formed on the first oxide film. Claim 20, line 4. The first oxide film debonds the metal film from the substrate. Claim 20, line 5. A second oxide layer is formed on the metal film. A

semiconductor film is formed on the second oxide film in which the semiconductor film has a first level of transistors and a second level of transistors in the Z-dimension. Claim 20, lines 7-10.

Horiba relates to low resistance ground wiring in a semiconductor device. More specifically, *Horiba* relates to fabricating a semiconductor device that includes a first insulating film formed partially on the semiconductor substrate. Gate electrodes are formed on the first insulating film. *Horiba*, col. 4, lines 15-16. A diffusion layer is then formed at a surface of the semiconductor substrate around the gate electrodes. *Horiba*, col. 4, lines 20-21. An insulating sidewall film is formed around a sidewall of the gate electrodes. *Horiba*, col. 4, lines 22-23. A third insulating film is partially covering the semiconductor substrate, the insulating sidewall film, and the gate electrodes so that the diffusion layer, a part of the gate electrodes, and a top edge of the insulating sidewall film are exposed. *Horiba*, col. 4, lines 23-27. A second conductive film covers the third insulating film, the exposed part of the gate electrodes, the exposed top edge of the insulating sidewall film and the semiconductor substrate. *Horiba*, col. 4, lines 27-31. A third conductive film covers the second conductive film. *Horiba*, lines 1-32. A fourth insulating film has a planarized top surface at such a level that a top surface of the third conductive film is exposed. *Horiba*, lines 32-33. A fourth conductive film bridging over the top surface of the third conductive film. *Horiba*, lines 33-35. The fourth conductive film, the fourth insulating film, the third conductive film and the second conductive film cooperate with one another to form a ground wiring layer." *Horiba*, col. 4, lines 35-38. *Horiba* fails to disclose a "semiconductor film having a

first level of transistors and a second level of transistors made of single crystal silicon" as in claim 20, lines 7-10. Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) to claim 20. Since claim 21 depends from claim 20, claim 21 has at least the limitations of claim 20. Claim 21, therefore, is also not anticipated by *Horiba* for at least the reasons that claim 20 is not anticipated by *Horiba*.

For the above-stated reasons, Applicant asserts that claims 20-21 are not anticipated by the *Horiba*. Applicant respectfully requests that the Examiner withdraw the rejection to claims 20-21 under 35 U.S.C. § 102(b).

B. 35 U.S.C. § 103(a): Rejection of Claims 14 and 17-22

The Examiner rejects claims 14 and 17-22 under 35 U.S.C. § 103(a) as being unpatentable over *Horiba*. Claim 14 relates to an apparatus comprising a first substrate with a semiconductor film formed thereon wherein the semiconductor film is demarcated from the rest of the first substrate by a damaged surface.

Horiba fails to teach or suggest all of the elements of claim 14. For example, *Horiba* fails to teach or suggest the use of a damaged surface. See claim 1, lines 3-4. If the Examiner believes that *Horiba* teaches this feature, Applicant requests that the Examiner provide a precise citation to support such an assertion.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any fees due in connection with the filing of this response, please

charge those fees to our Deposit Account No. 02-2666. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 10/20/00

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail No. EM560646634US in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on October 20, 2000.

Nadya Gordon 10/20/00
Nadya Gordon *Date*